

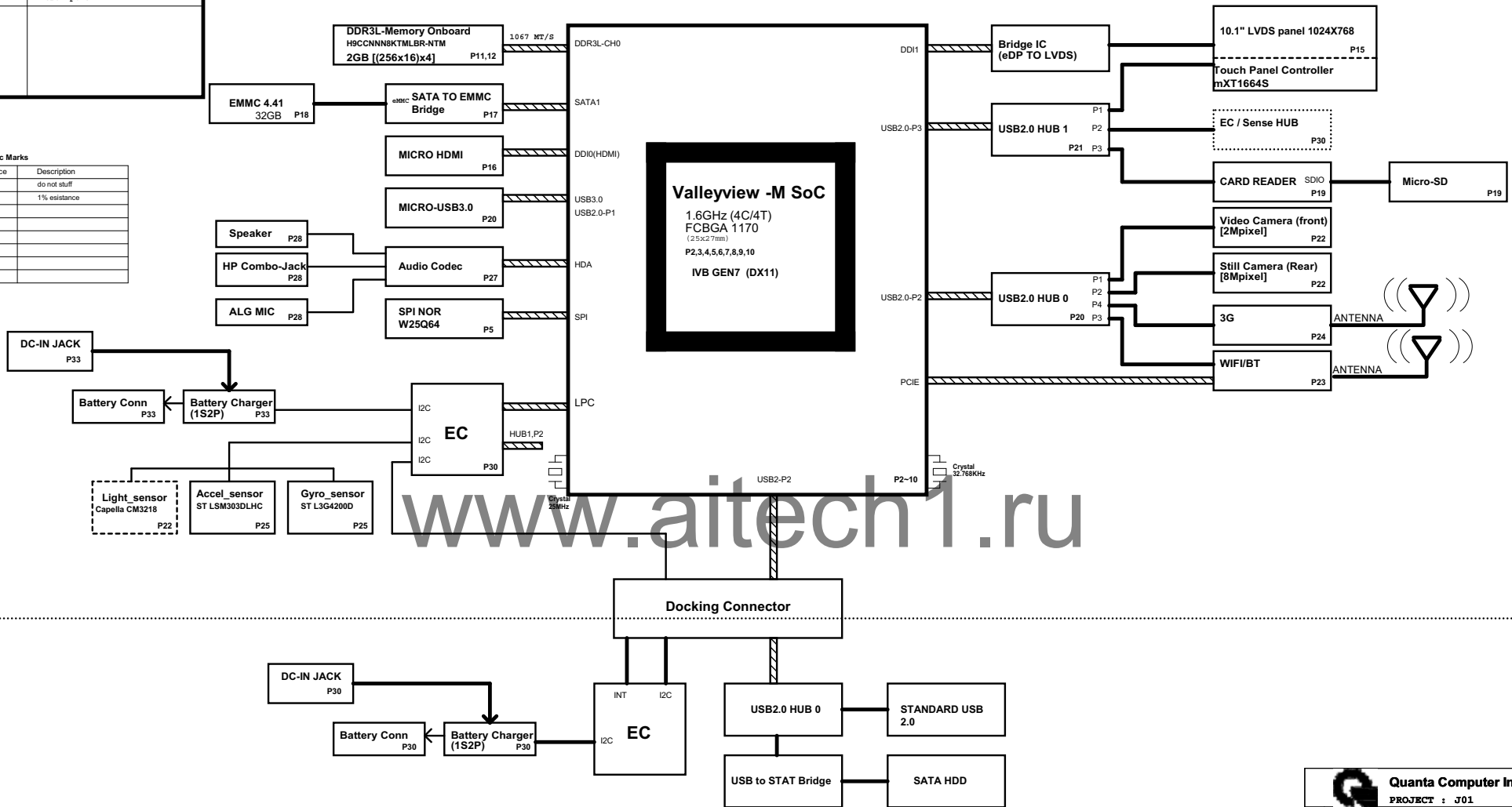
VER : 1A

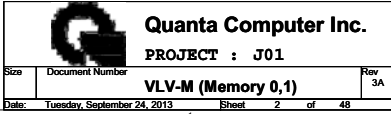
Block Diagram (Intel Bay Trail-M Platform)

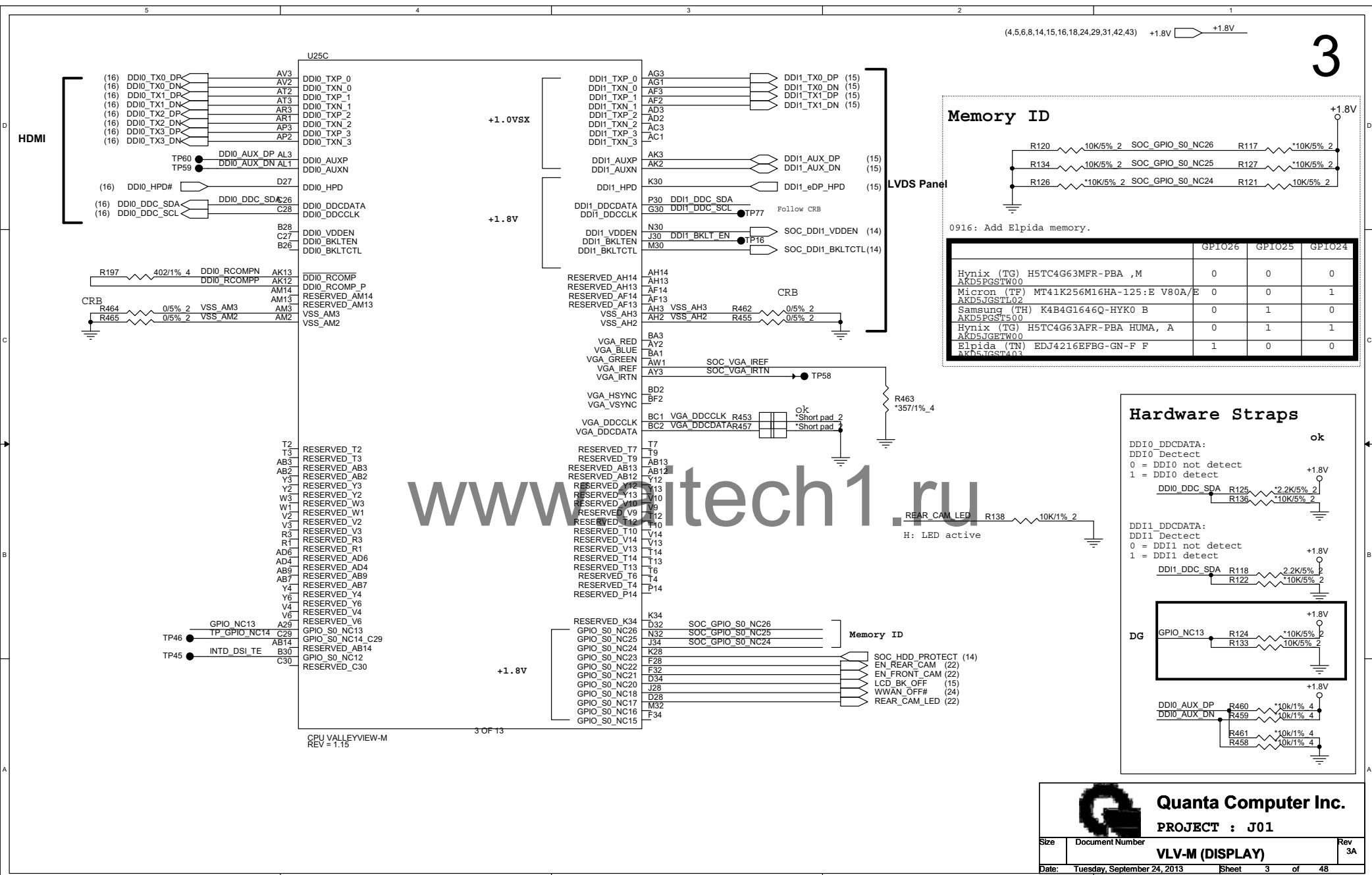
01

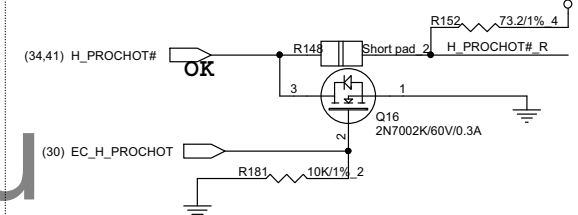
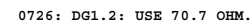
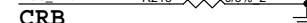
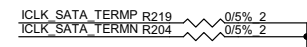
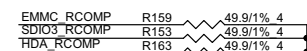
Schematic Marks

Reference	Description
*	do not stuff
1F	1% resistance

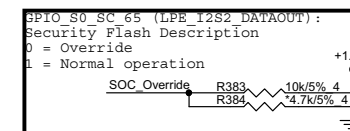








```
GPIO_S0_SC_63 (LPE_I2S2_FRM):
BIOS/EFI Boot Selection
0 = LPC
1 = SPI
```

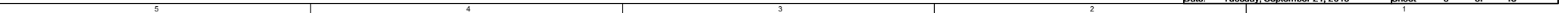
**VLV-M (SATA/PCIE&AUDIO)**

Size	Document Number	Rev
	VLV-M (SATA/PCIE&AUDIO)	3A
Date:	Tuesday, September 24, 2013	Sheet 4 of 48

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Date: Tuesday, September 24, 2013 Sheet 7 of 48



Size	Document Number	Rev
	VLV-M (POWER 2/2)	3A
Date:	Tuesday, September 24, 2013	Sheet 8 of 48

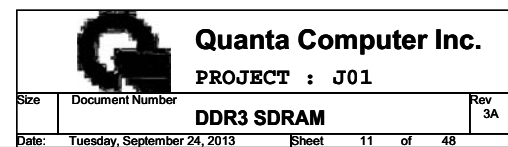
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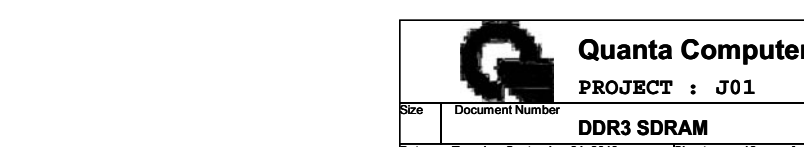


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PROJECT : J01

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VLV-M SOC (DEBUG)		
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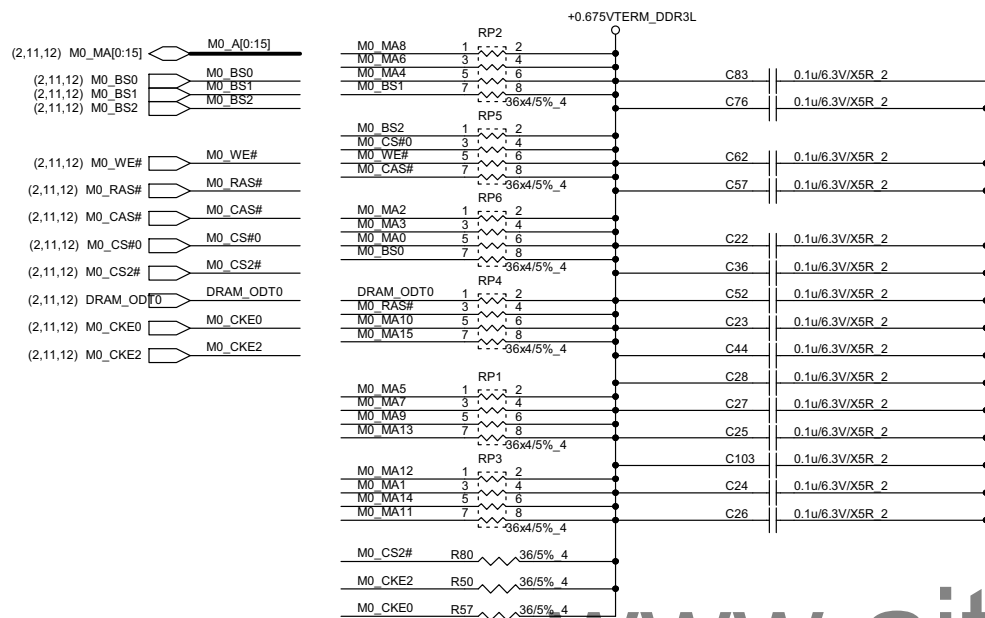




CH0 Address/Control/Clock Terminations

(2,35,43) +0.675VTERM_DDR3L  +0.675VTERM_DDR3L

13



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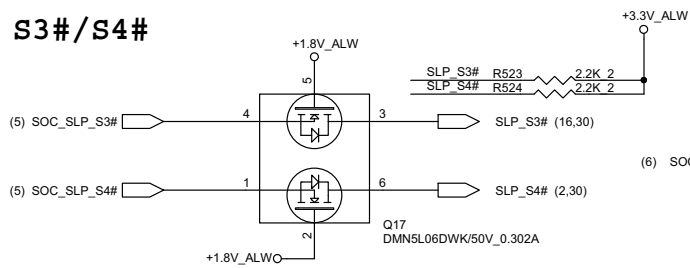
Quanta Computer Inc.
PROJECT : J01

Size	Document Number	Rev
		3A
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Sheet 13 of 48		

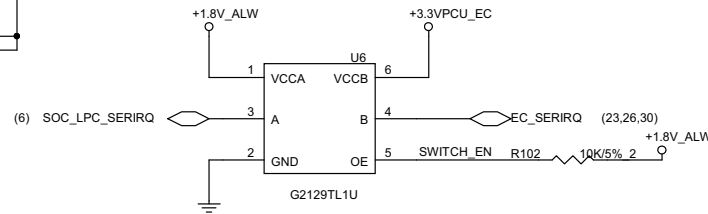
DDR3 TERMINATION

Level Shifter

S3#/S4#

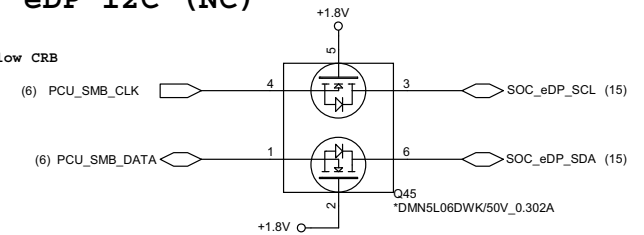


SERIRQ

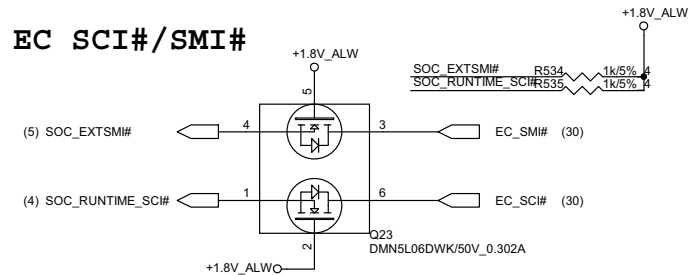


eDP I2C (NC)

Follow CRB

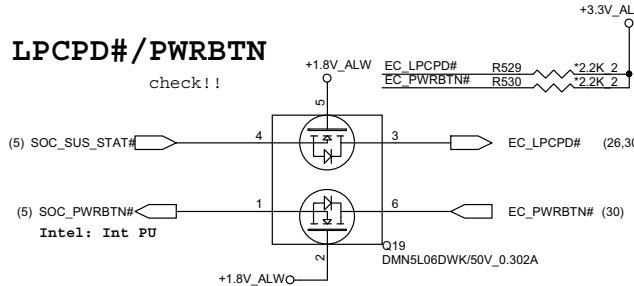


EC SCI#/SMI#

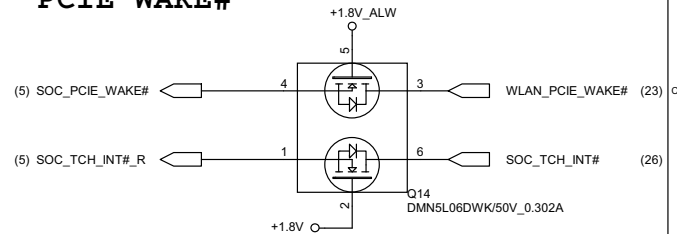


LPCPD#/PWRBTN

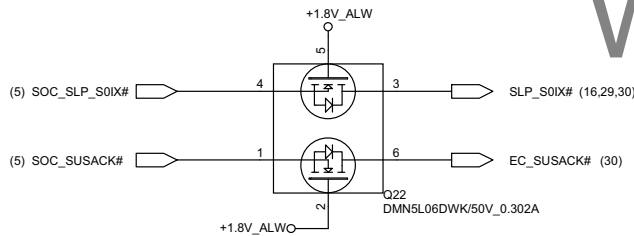
check !



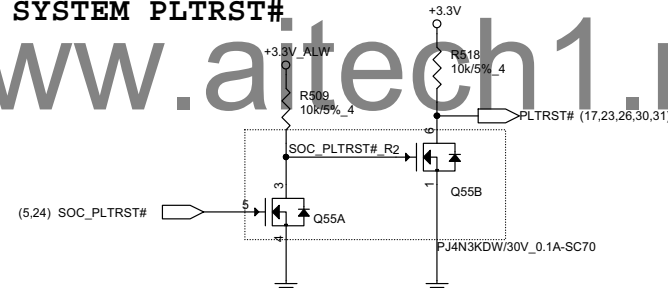
PCIE WAKE#



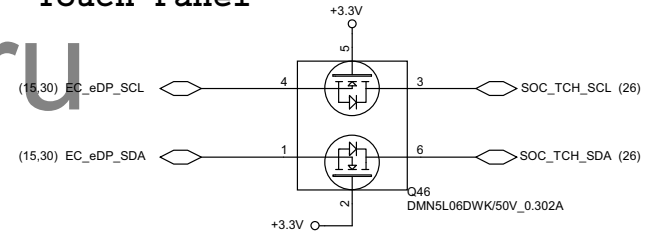
SLP_S0IX#/SOC_SUSACK#



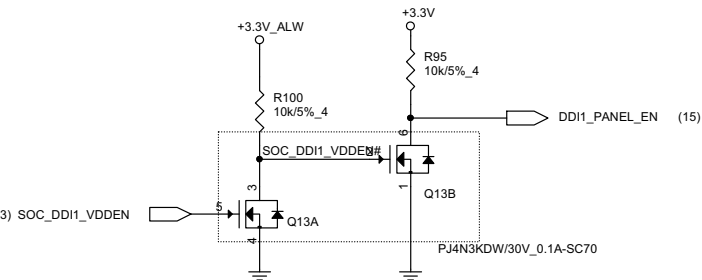
SYSTEM PLTRST#



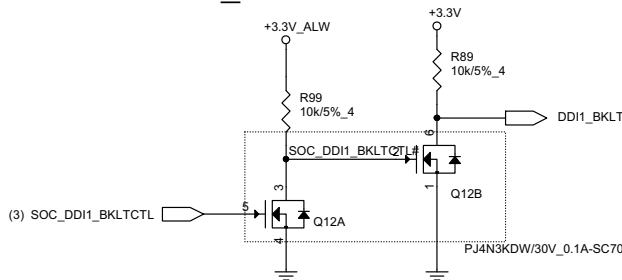
Touch Panel



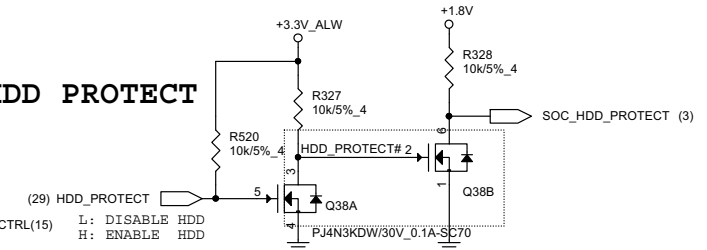
PANEL POWER ON



PANEL BKLT_CTRL



HDD PROTECT

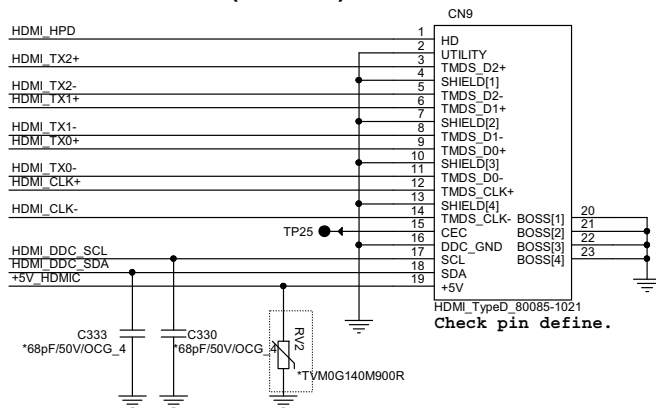


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PROJECT : J01

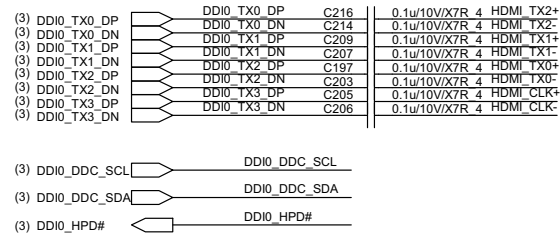
Size	Document Number	Rev
	LEVEL SHIFTERS	3A
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HDMI CONNECTOR (D TYPE)

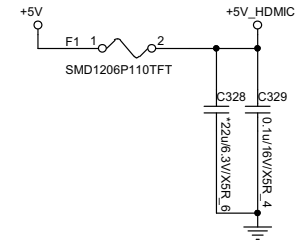


HDMI INTERFACE

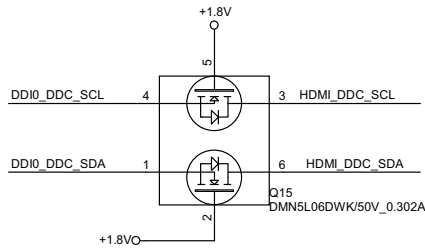
DG MAPPING OK



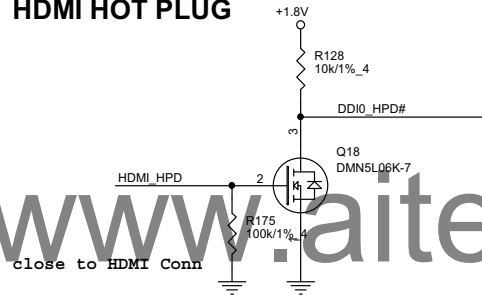
HDMI POWER SUPPLY



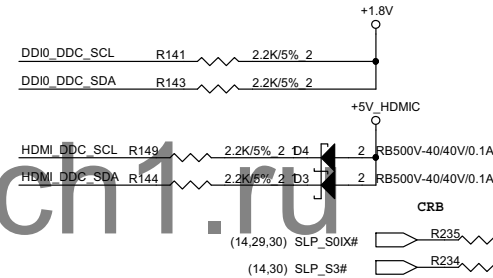
I2S BUS LEVEL SHIFT



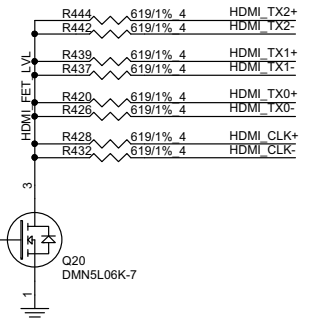
HDMI HOT PLUG



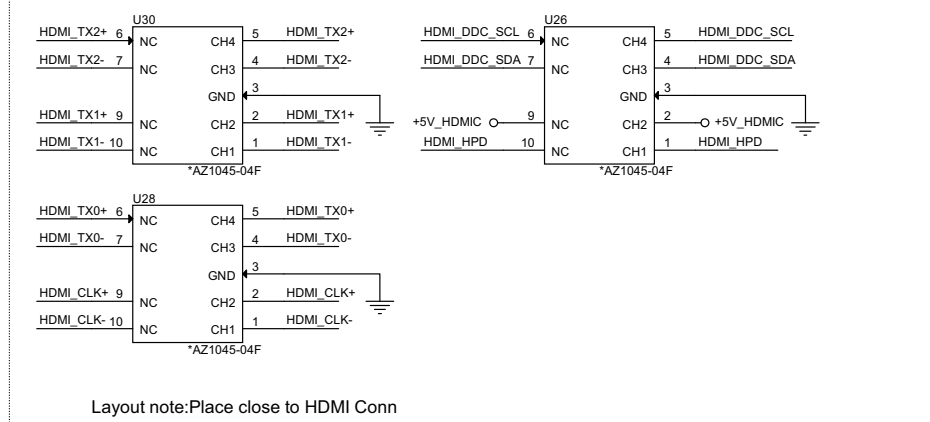
I2C Pull up



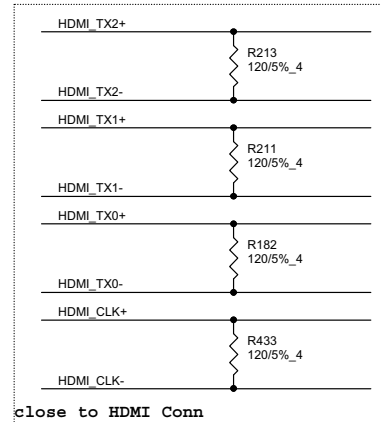
HDMI LEVEL SHIFT



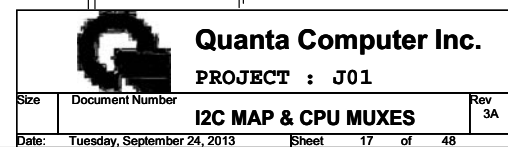
ESD reserve for HDMI



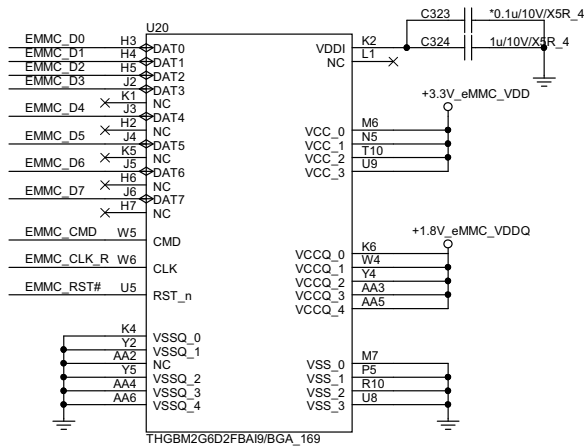
EMI reserve for HDMI



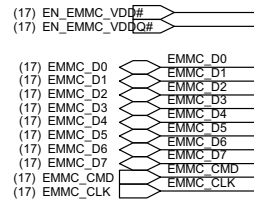
17



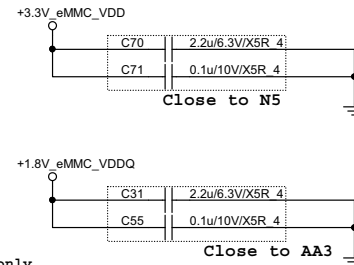
eMMC



Interface

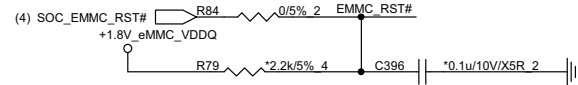


eMMC Power

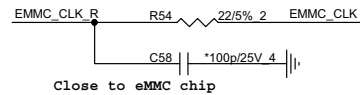


eMMC RST#

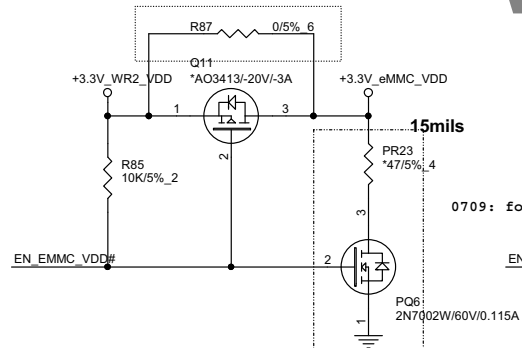
0709: for eMMC only



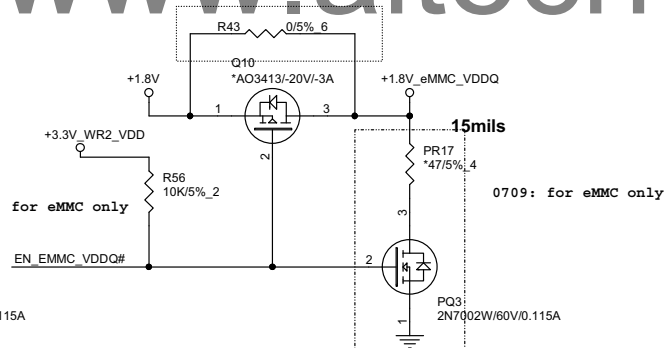
eMMC CLOCK



eMMC VDD POWER CONTROL



eMMC VDDQ POWER CONTROL



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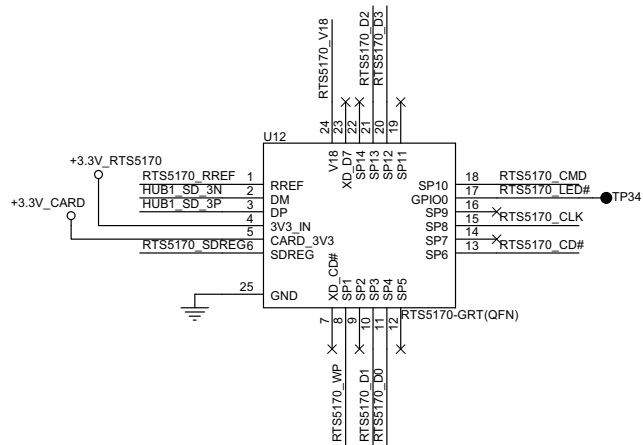


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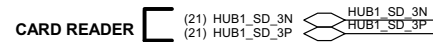
PROJECT : J01

Size	Document Number	Rev
	Touch screen	3A
Date:	Tuesday, September 24, 2013	Sheet 18 of 48

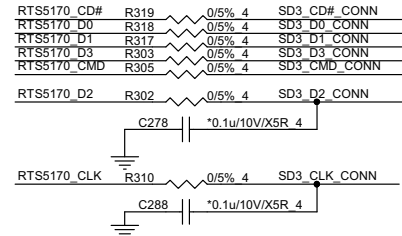
Mirco SD



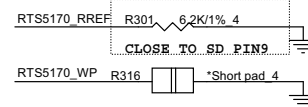
CARD PCIE INTERFACE



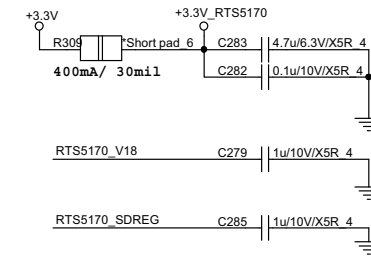
CO-LAY with SoC



HW STRAPS

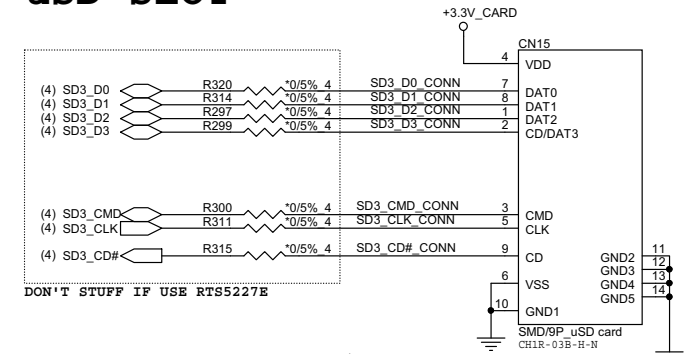
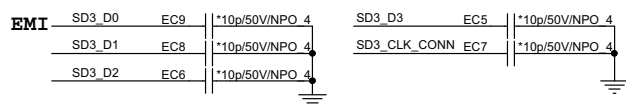
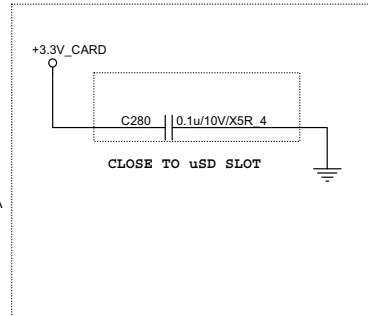
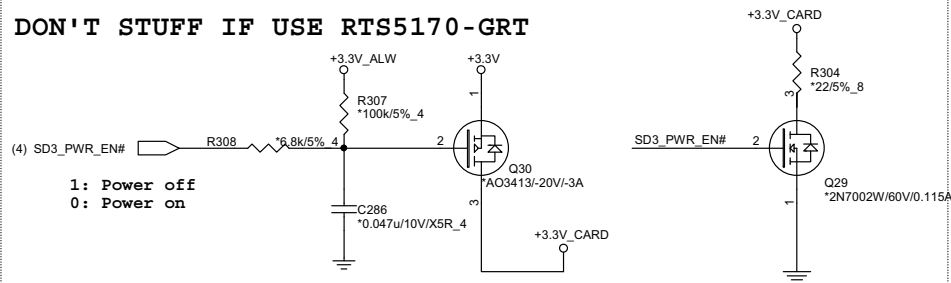


CARD POWER



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DON'T STUFF IF USE RTS5170-GRT



0618: change p/n DFHD09MR120



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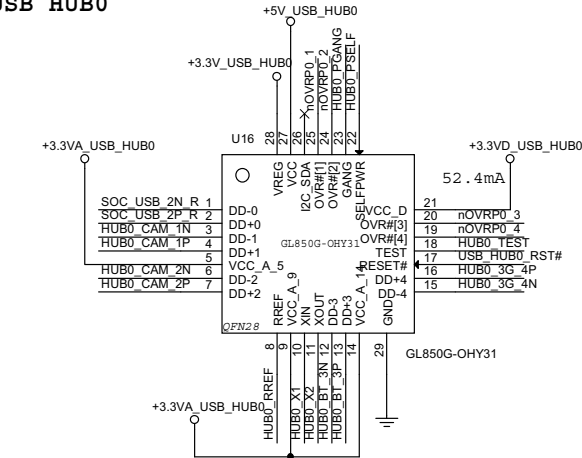
PROJECT : J01

Ext. uSD

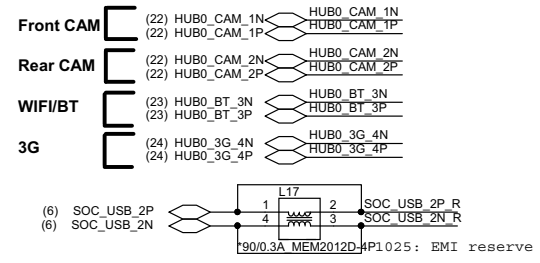
Size	Document Number	Rev
	Ext. uSD	3A
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Date: Tuesday, September 24, 2013 Sheet 19 of 48

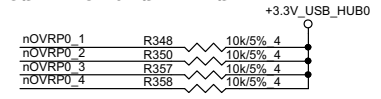
USB HUB0



USB HUB0 Interface



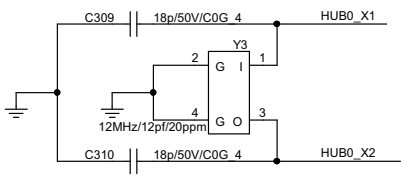
USB HUB0 STRAPS



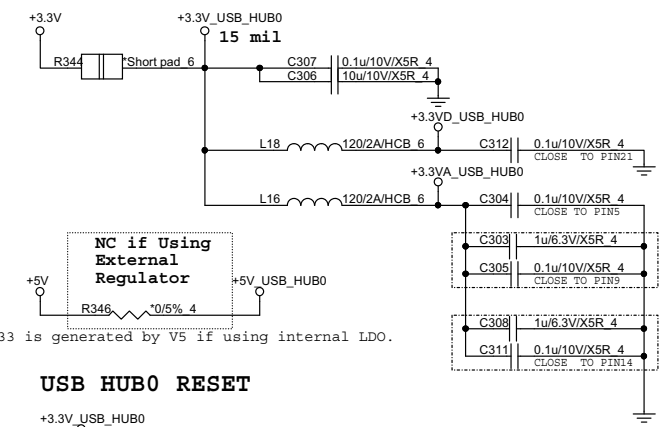
HUB PSELF
0: GL850G is bus-powered
1: GL850G is self-powered

HUB TEST
0: Normal Operation (Internal PD)
1: Test Mode

USB HUB0 XTAL

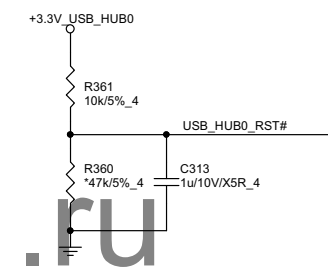


USB HUB0 Power



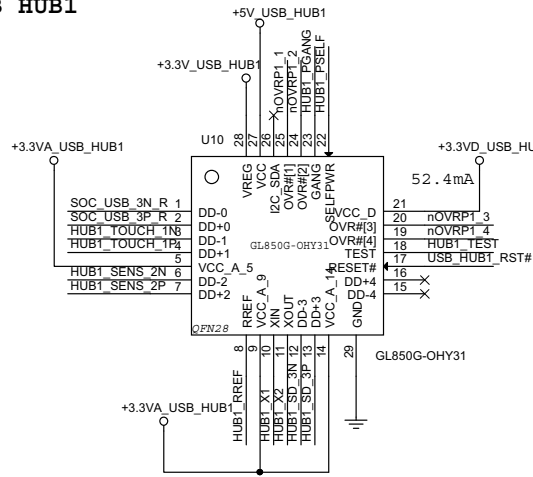
On HUB IC, V33 is generated by V5 if using internal LDO.

USB HUB0 RESET

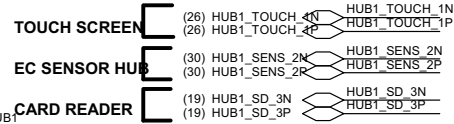


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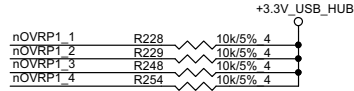
USB HUB1



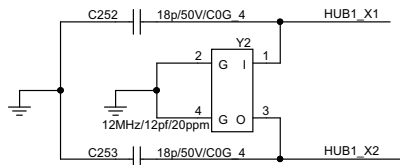
USB HUB1 Interface



USB HUB1 STRAPS

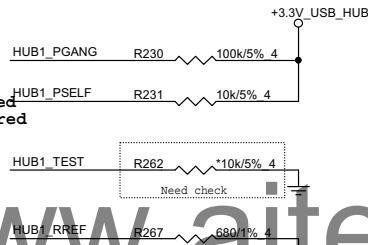


USB HUB1 XTAL

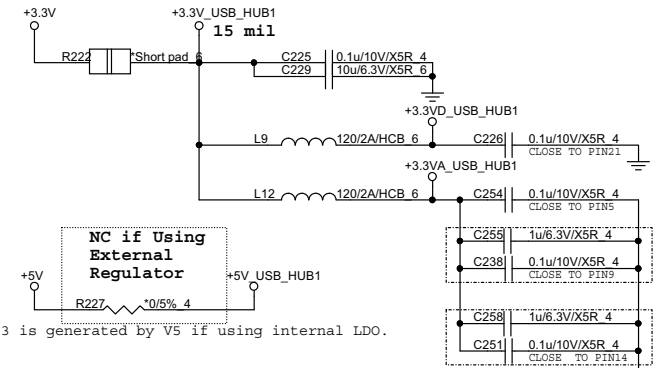


HUB PSELF
0: GL850G is bus-powered
1: GL850G is self-powered

HUB TEST
0: Normal Operation (Internal PD)
1: Test Mode

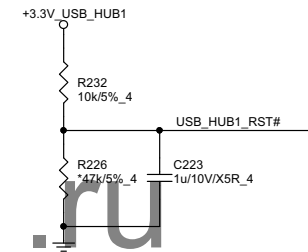


USB HUB1 Power



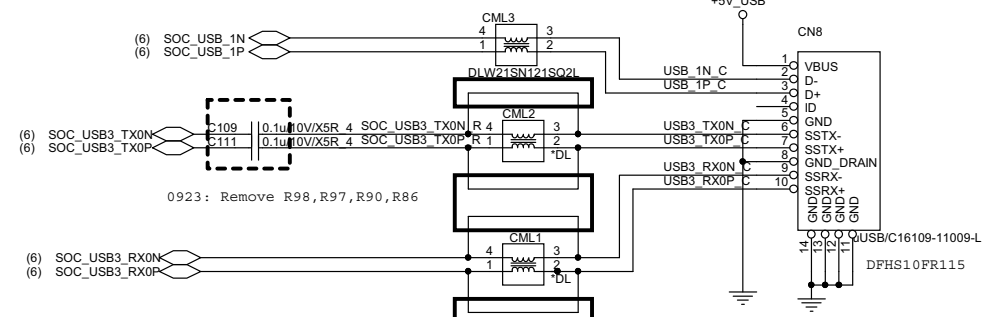
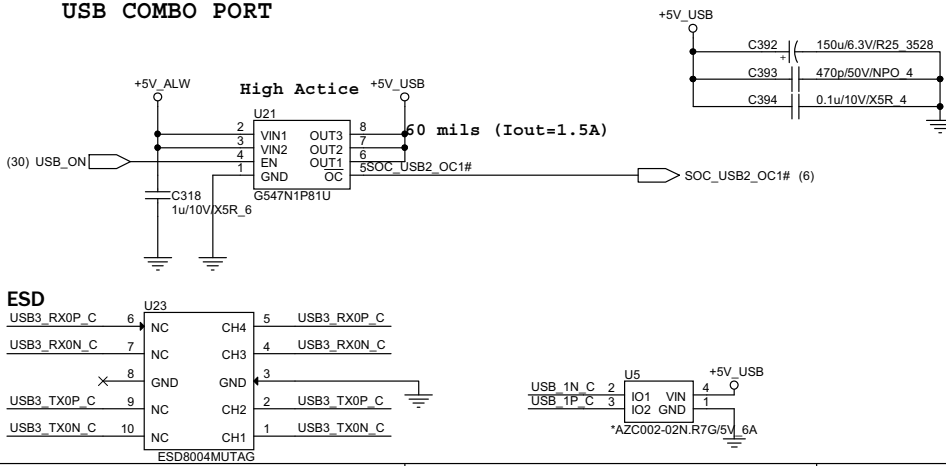
On HUB IC, V33 is generated by V5 if using internal LDO.

USB HUB RESET



USB COMBO PORT

0603: change footprint



Use USB3.0 common mode choke different with USB2.0



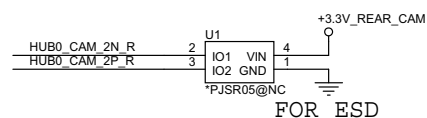
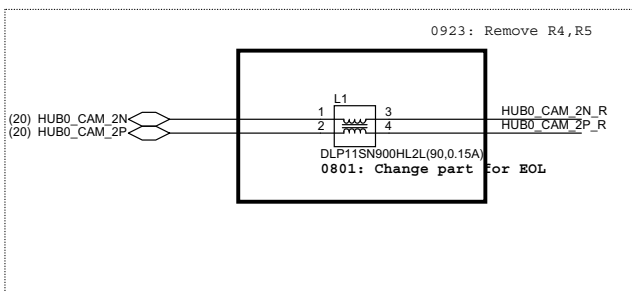
Quanta Computer Inc.

PROJECT : J01

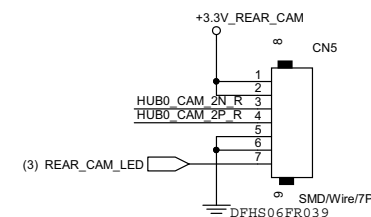
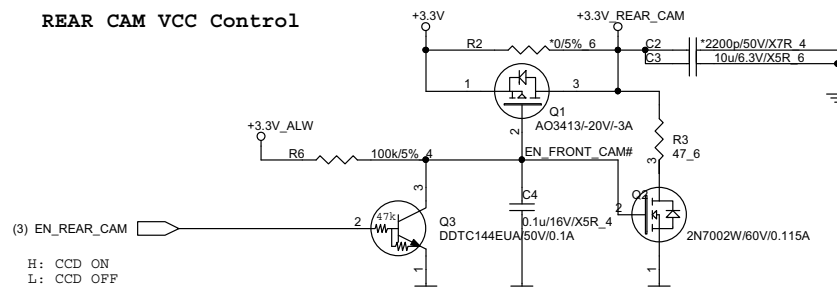
USB HUB1 / COMBO 3.0

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		3A
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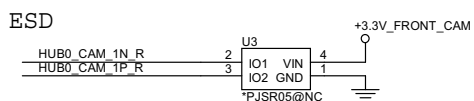
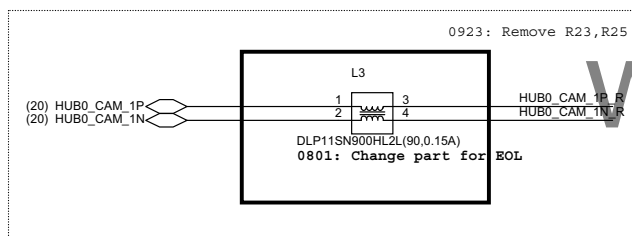
REAR CCD 8M



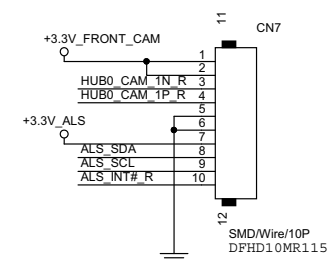
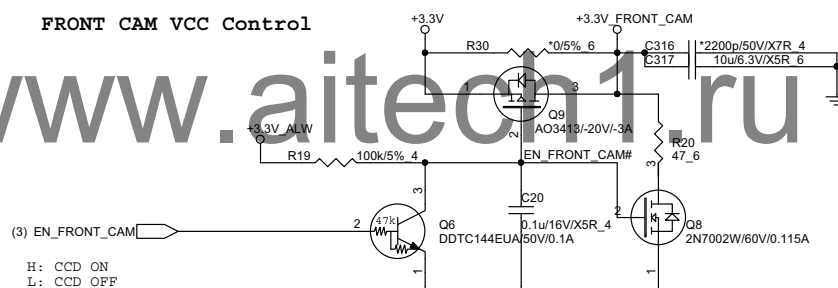
REAR CAM VCC Control



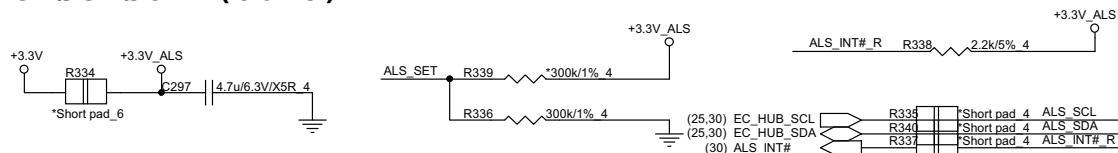
Front CCD 2M



FRONT CAM VCC Control



G-Sensor (0823)



I2C Address Setting :

R339	R336	I2C Address
asm		0x48
asm		0x10



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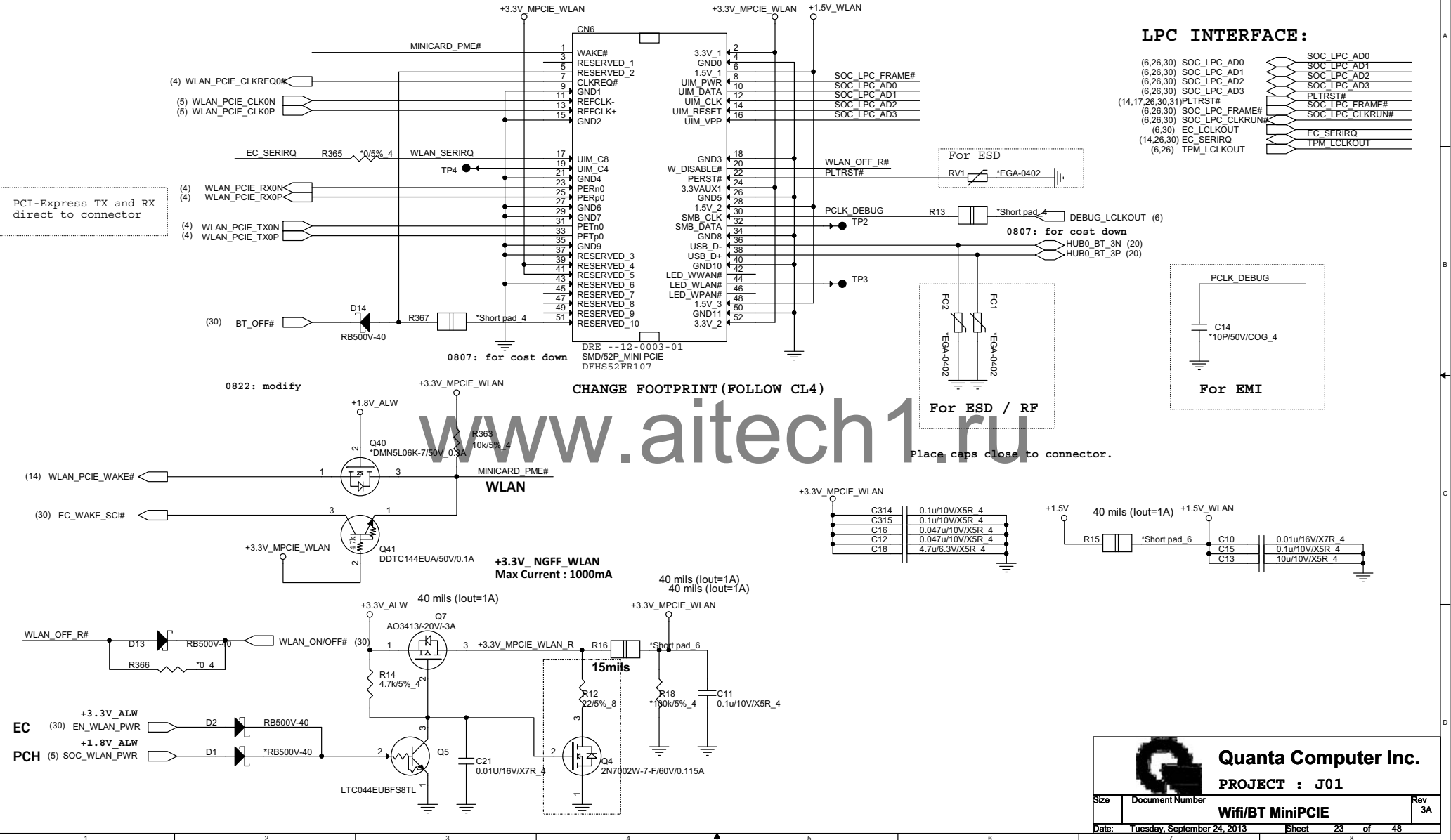
Size	Document Number	Rev
		3A

2M/8M CCD&Flash LED

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Mini PCIE Wifi/BT connector

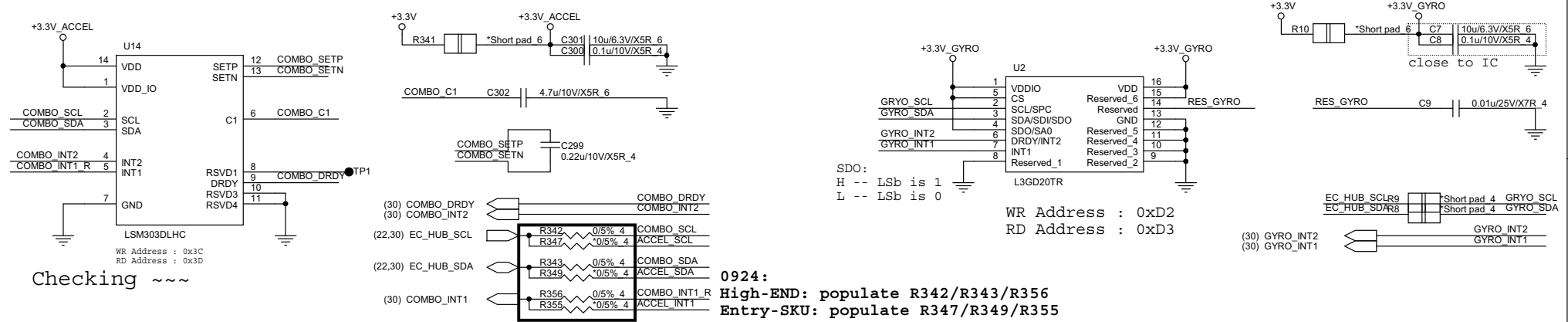
22



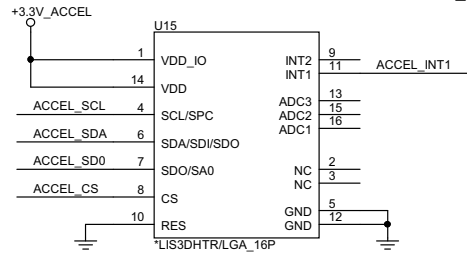
Quanta Computer Inc.
PROJECT : J01

Size	Document Number	Rev
		3A
Date:	Tuesday, September 24, 2013	Sheet 23 of 48

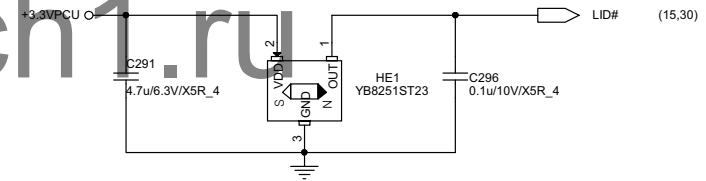
G-sensor/E-compass/Magnetometer (High-end SKU) Gyroscope (High-end SKU) 25



Accelerometer (Entry SKU)



Hall sensor

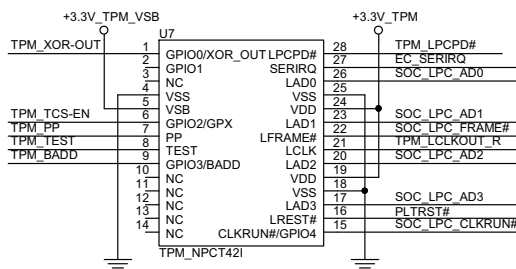


Quanta Computer Inc.

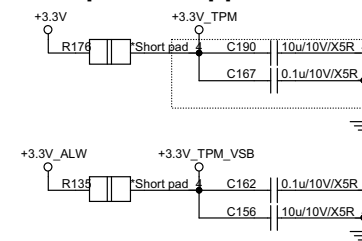
PROJECT : J01

Size	Document Number	Rev
	GPS SAR LED ALS POWER BUTTON	3A

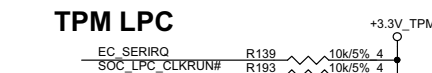
Date: Tuesday, September 24, 2013 Sheet 25 of 48



TPM power supplier



TPM LPC

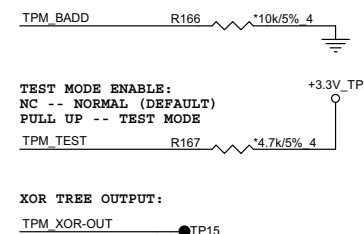


TPM HW STRAPS

```

BASE ADDRESS:
NC -- 7Eh-7Fh , NORMAL (DEFAULT)
PULL DOWN -- EEh-EFh

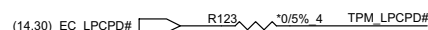
```



Signal	Pin(s)	Power Well	Type	Comments
LPCPD	28	V _{DD}	PU ₁₁₀	
GPIO4-0	15, 9, 6, 2, 1	V _{DD}	PU ₁₁₀	Programmable ¹
GPX	6	V _{DD}	PU ₁₁₀	Note ²
PP	7	V _{DD}	PU ₁₁₀ /PD ₁₁₀	Programmable ³
TEST	8	V _{DD}	PD ₁₁₀	Strap

1. Default at reset: GPIO0,2,3 enabled, GPIO1,4 disabled.
2. When GPIO-Express-00 (GPX) is selected for pin 6, the pull-up is enabled by default.
3. Default at reset: pull-down enabled.

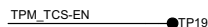
TPM LPCPD#



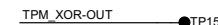
TPM PP



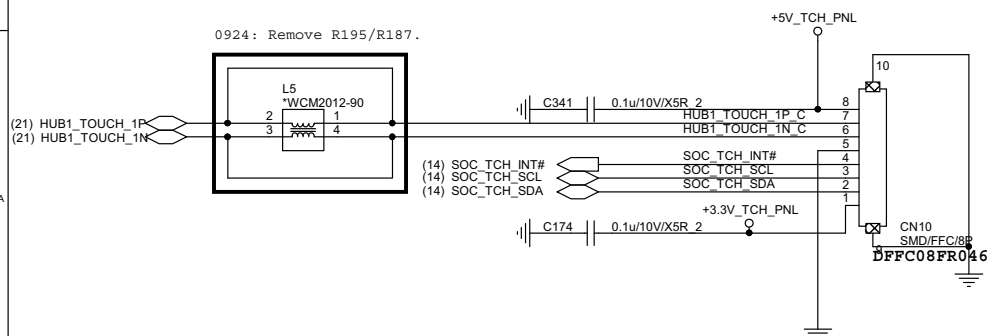
TPM TCS-EN



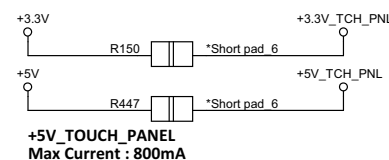
XOR TREE OUTPUT:



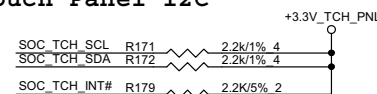
Touch Screen



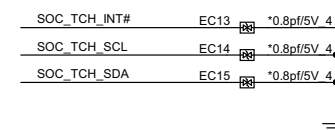
Touch Panel VCC Control



Touch Panel I2C



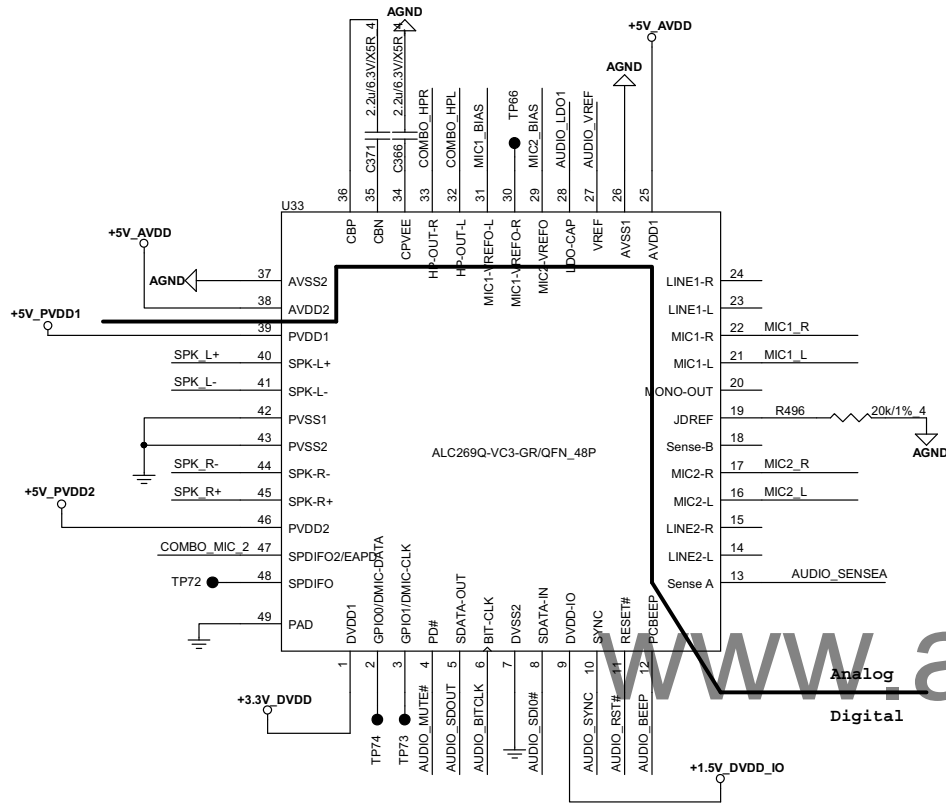
Touch Panel ESD



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PROJECT : J01

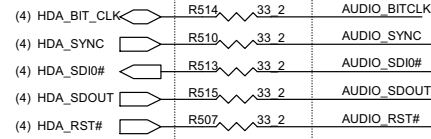
AUDIO CODEC

27



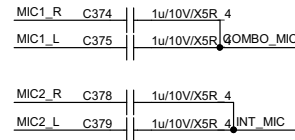
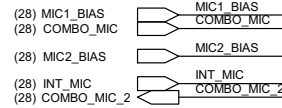
HDA:

Intel DG: 33 ohm

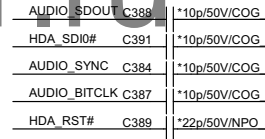
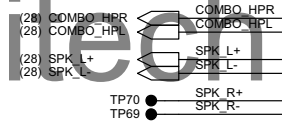


LAYOUT: CLOSE TO CODEC

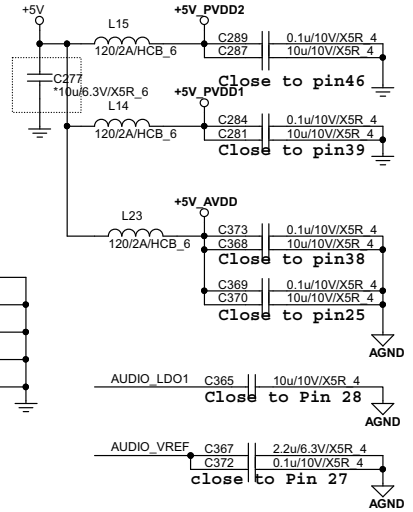
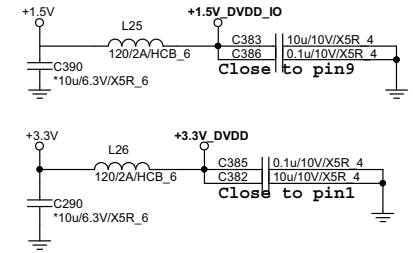
INT/EXT MIC:



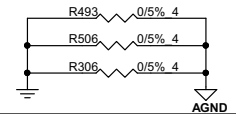
H/P OUT & SPK OUT:



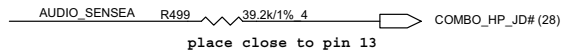
Audio Power



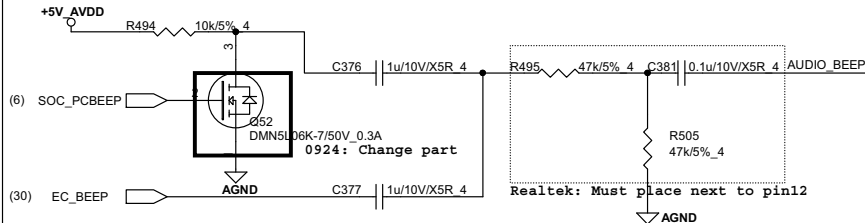
Analog Ground of Audio



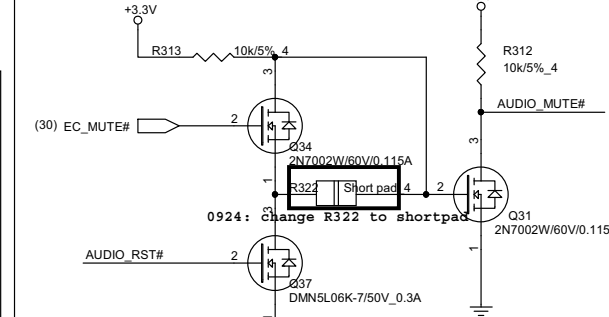
JACK SENSE



PC BEEP



AUDIO MUTE



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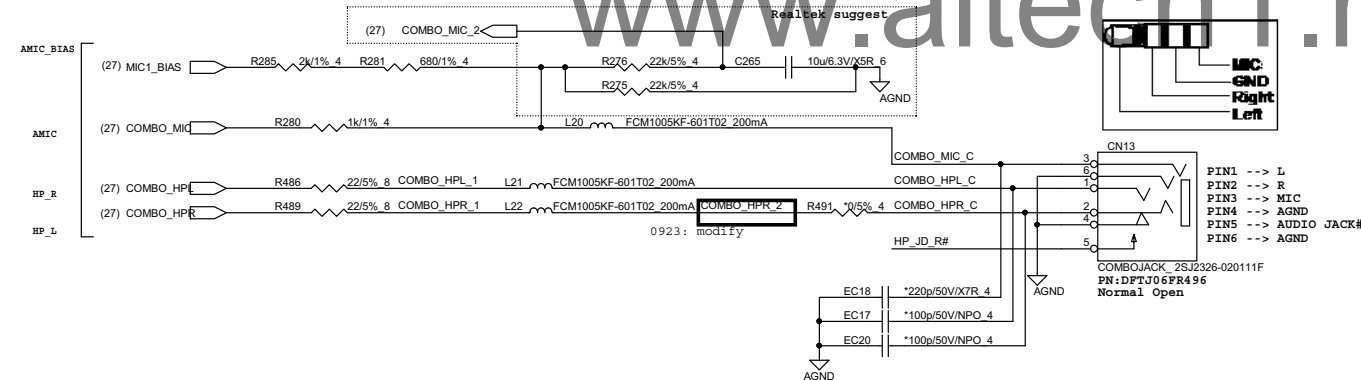
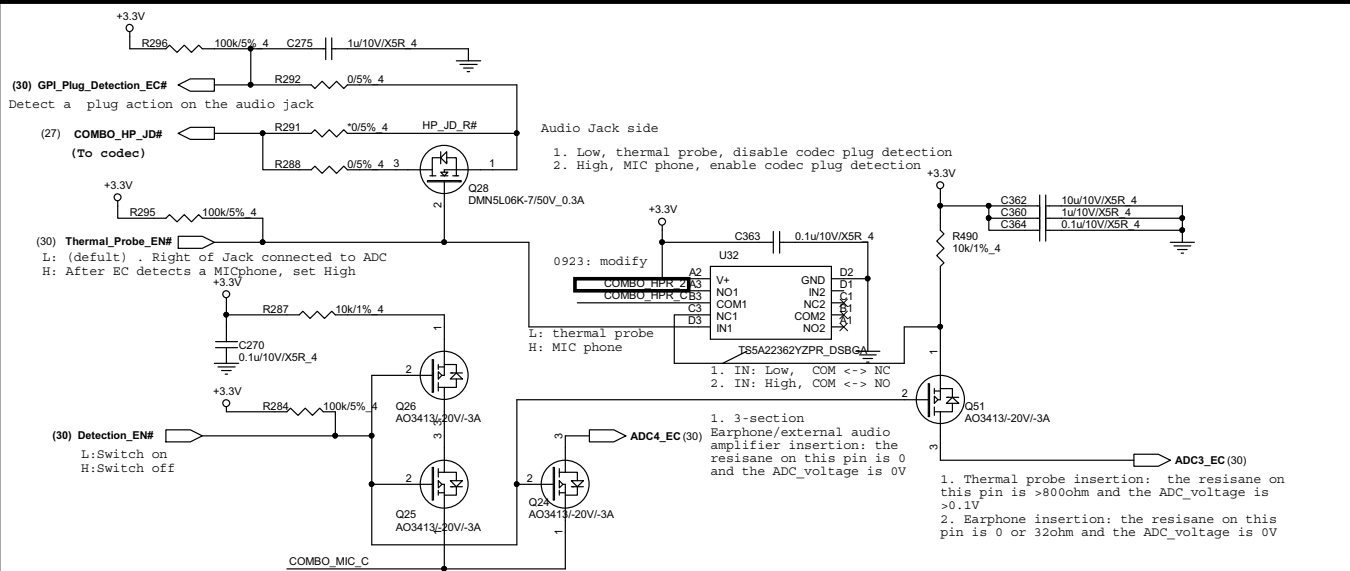
PROJECT : J01

HDA AUDIO CODEC ALC282

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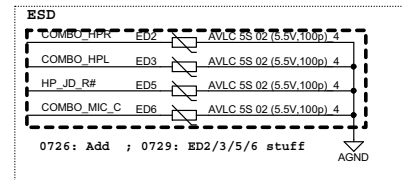
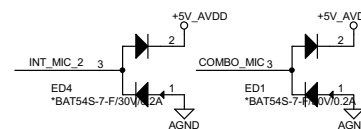
Headphone and Mic Jack

28



SPEAKERS

INTERNAL MIC

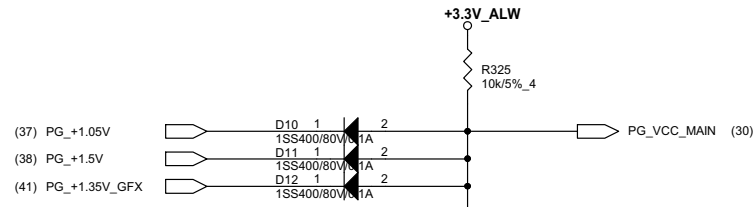
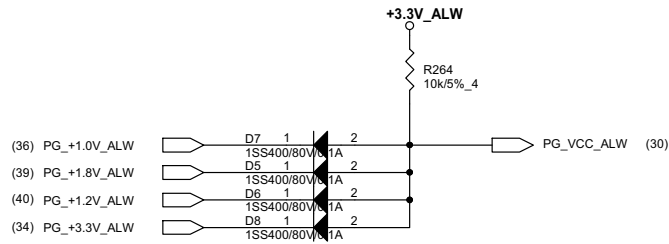


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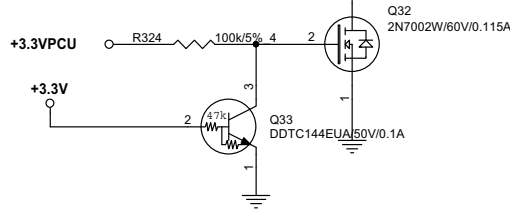
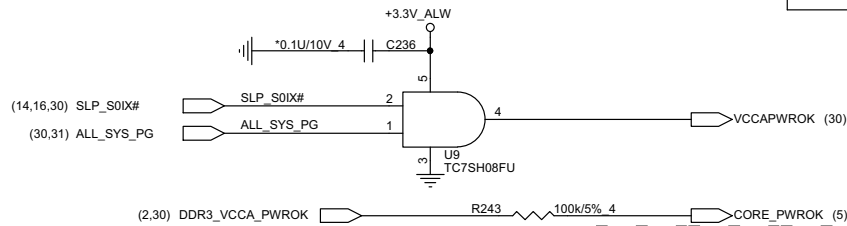
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ALWAYS POWER GOOD

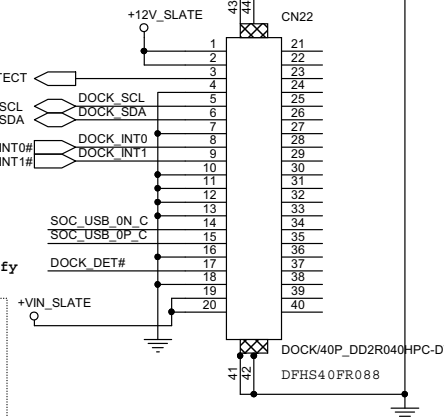
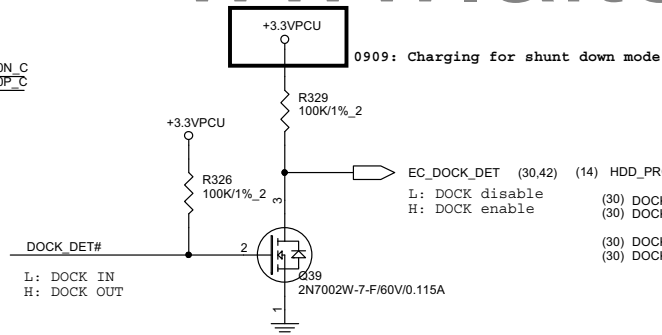
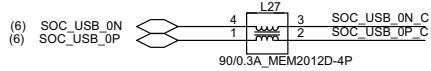
ALL SYSTEM POWER GOOD



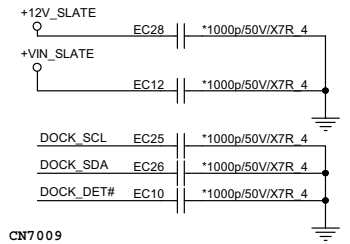
DRAM/CORE POWER OK



DOCKING CONNECTOR

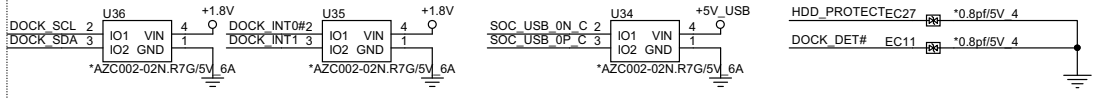


DOCK EMI



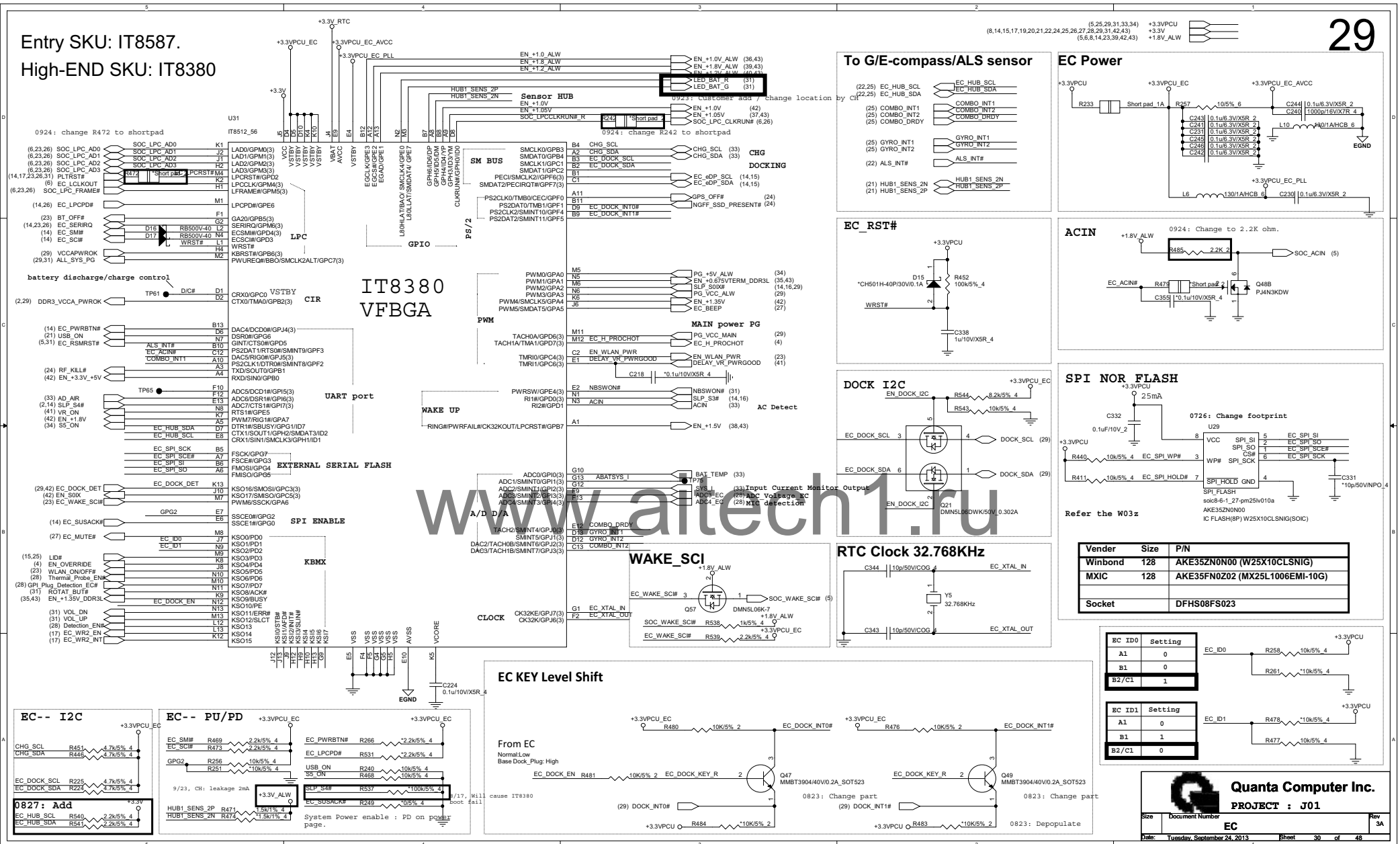
Close to CN7009

DOCK ESD



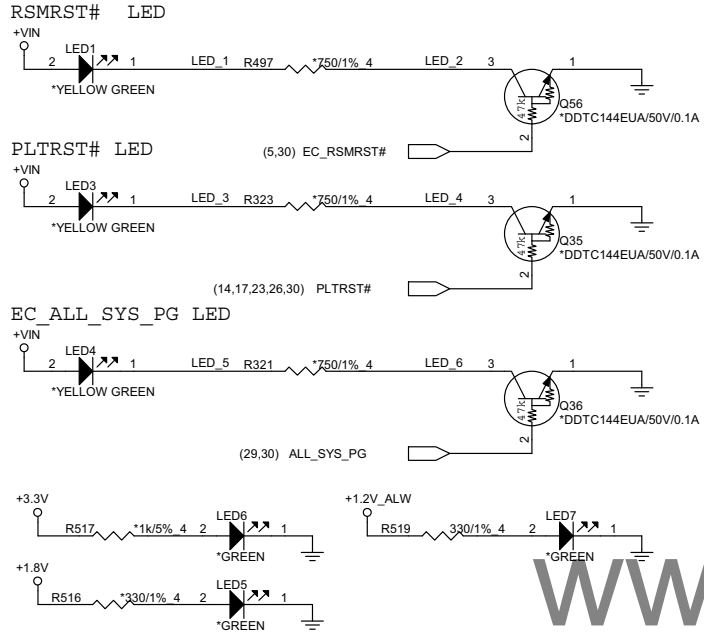
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Size	Document Number	Rev
	TBD	3A
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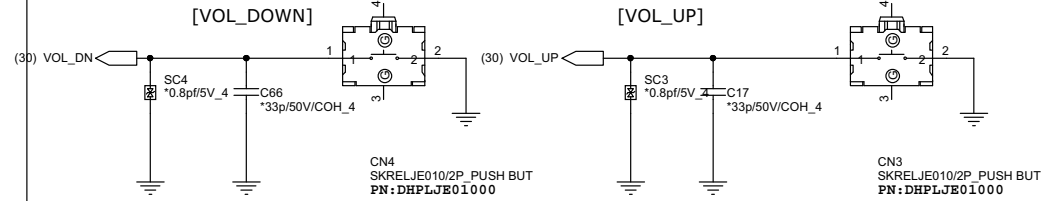


LED For bring-up

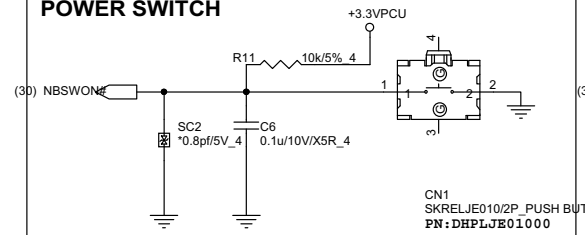
0914: Remove all from PVT2 stage



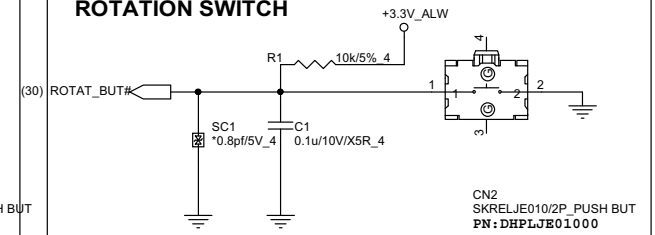
VOLUME CONTROL



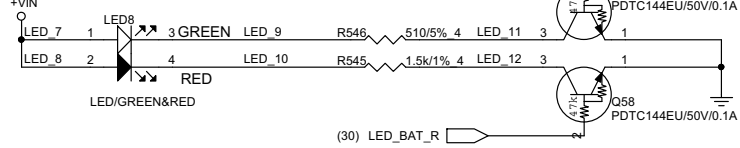
POWER SWITCH



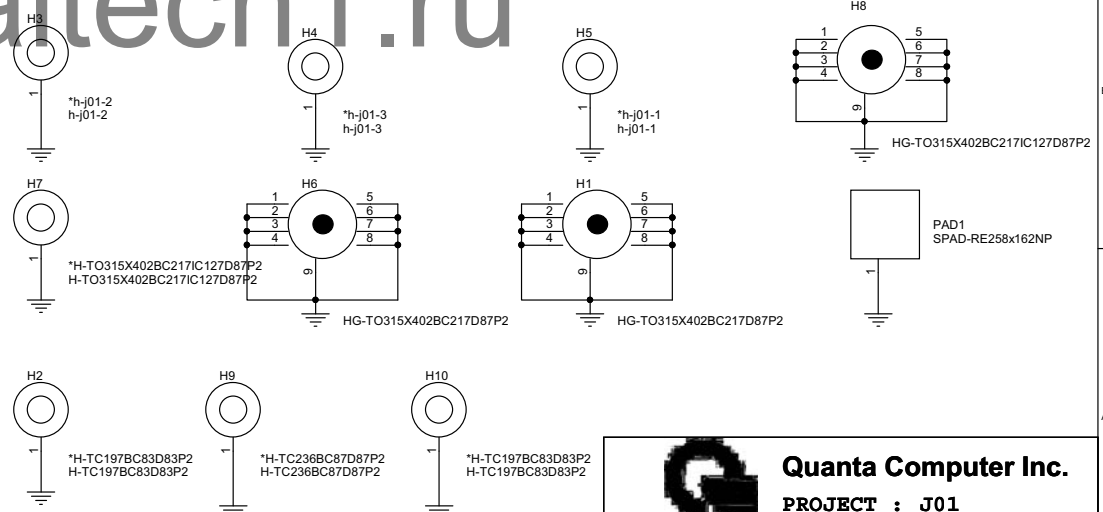
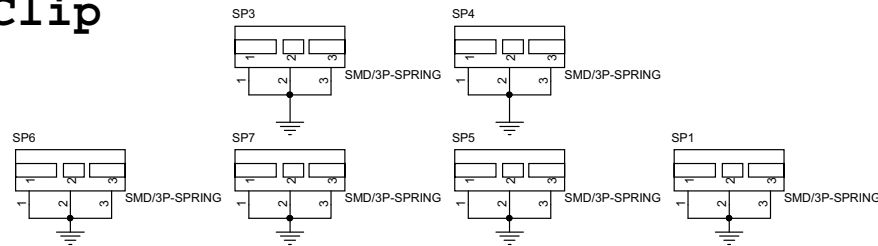
ROTATION SWITCH



0916: Customer request



Clip

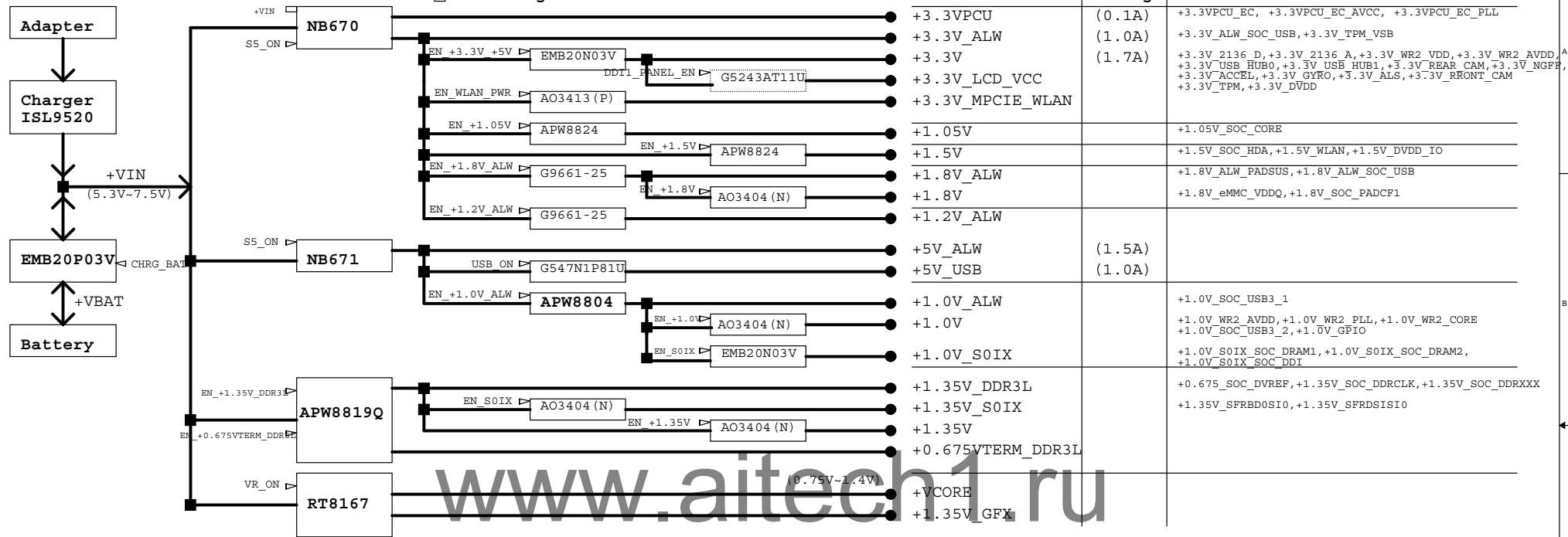


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	ULPMC	3A
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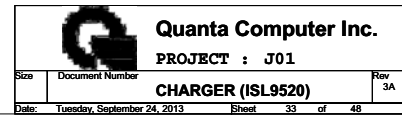
- ▷ Pink signals from EC
○ Blue signals from SOC
□ Black signals from others

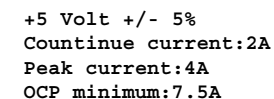


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POWER MAP		
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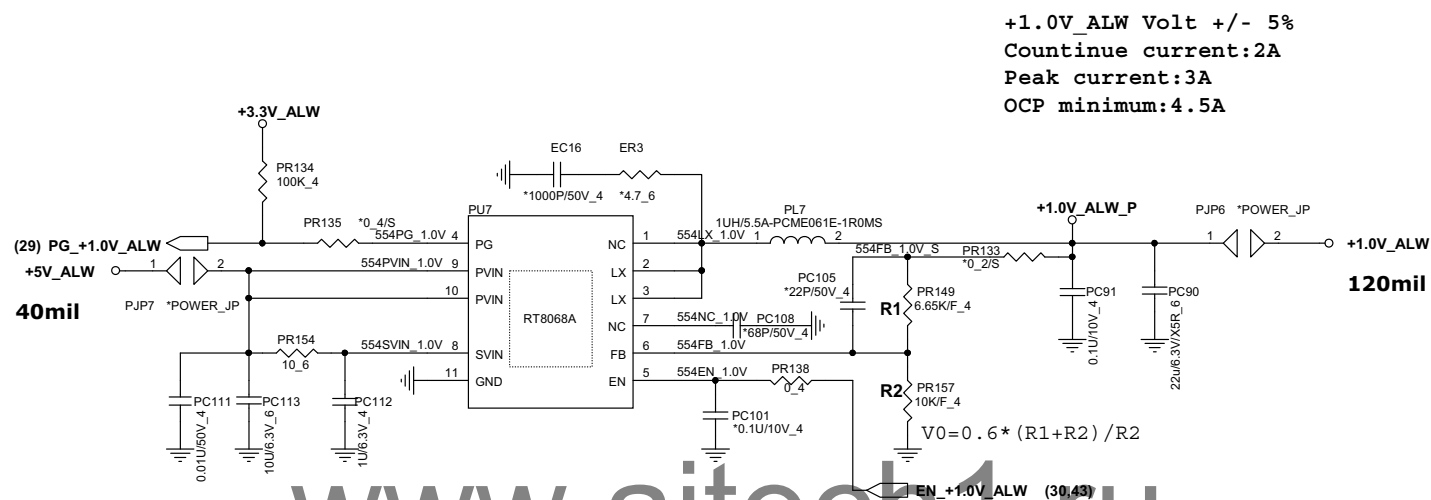


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3V/5V (TPS51123ARGER)

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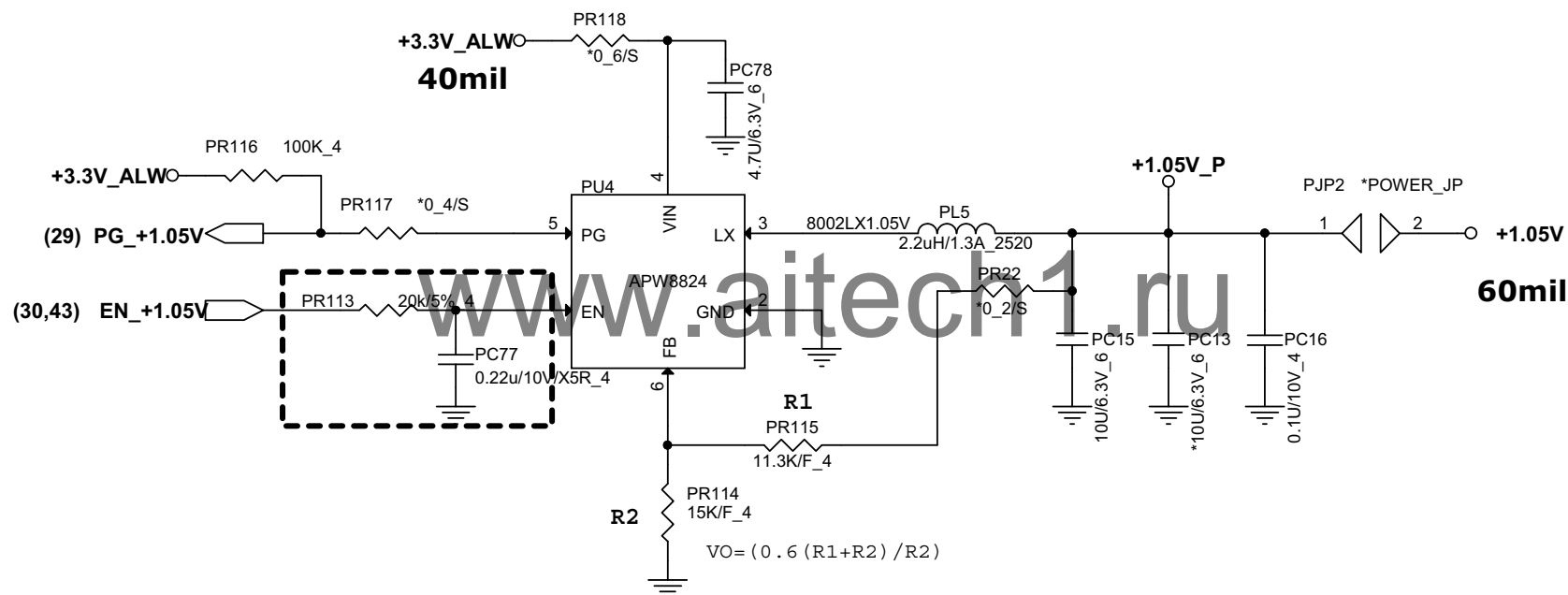
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	+1.0V_ALW(RT8068A)	3A
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+1.05V Volt +/- 5%
 Countinue current:1A
 Peak current:1.3A
 OCP minimum:2A



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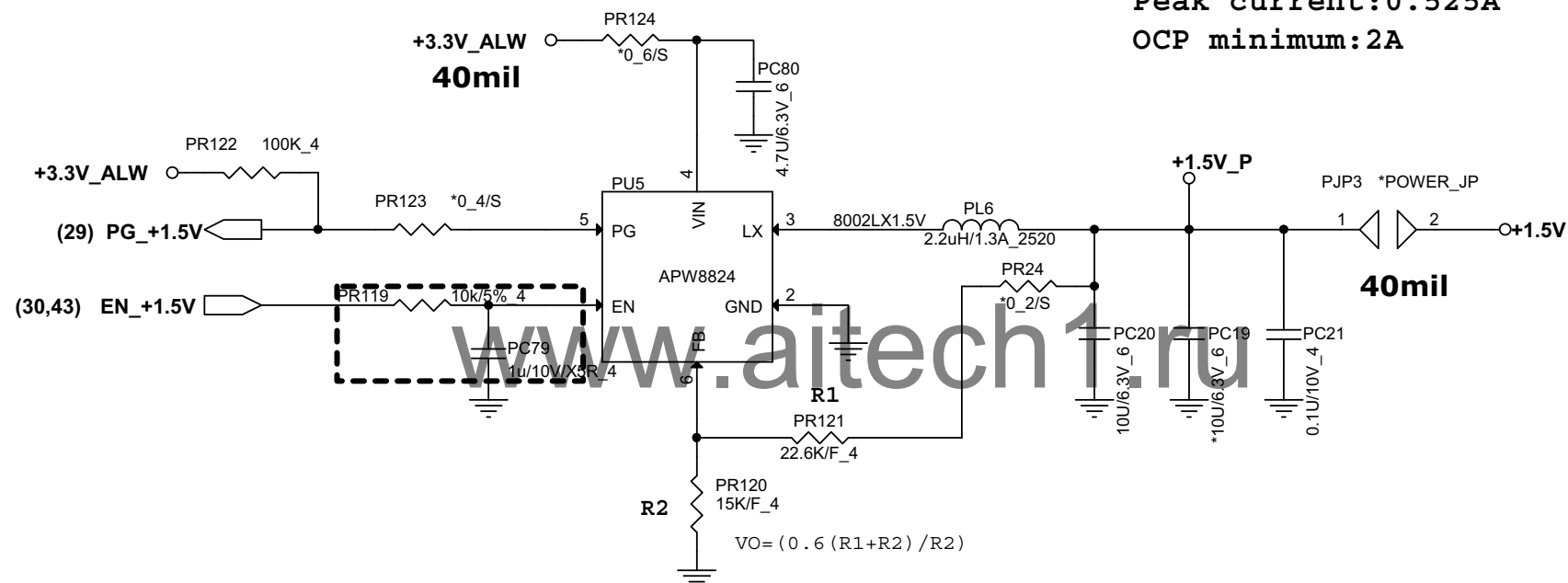
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+1.05V (APW8824)

Size	Document Number	Rev
		3A

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+1.5V +/- 5%
 Countinue current:0.45A
 Peak current:0.525A
 OCP minimum:2A



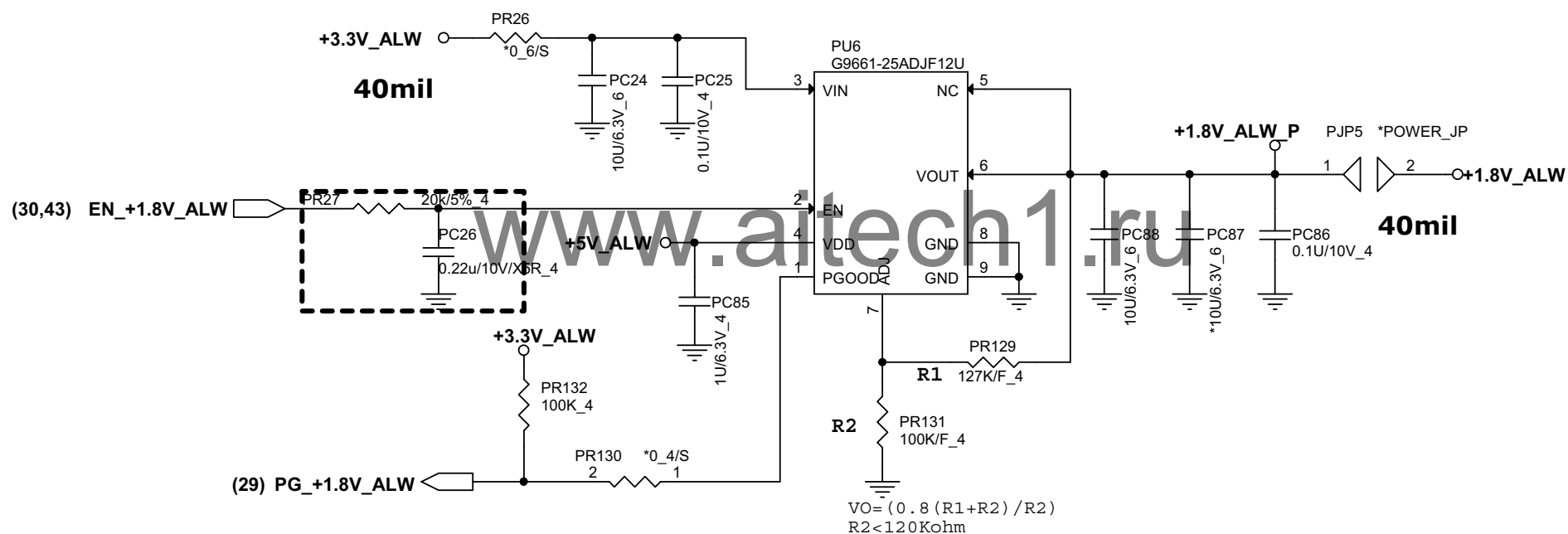
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	+1.5V (APW8824)	3A

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+1.8V Volt +/- 5%
 Countinue current:0.105A
 Peak current:0.3A



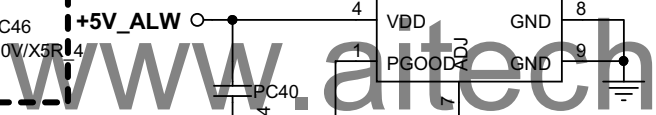
Quanta Computer Inc.

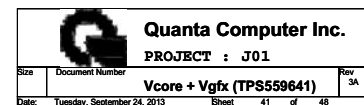
PROJECT : J01

Size	Document Number	Rev
	+1.8V_ALW(G9661)	3A

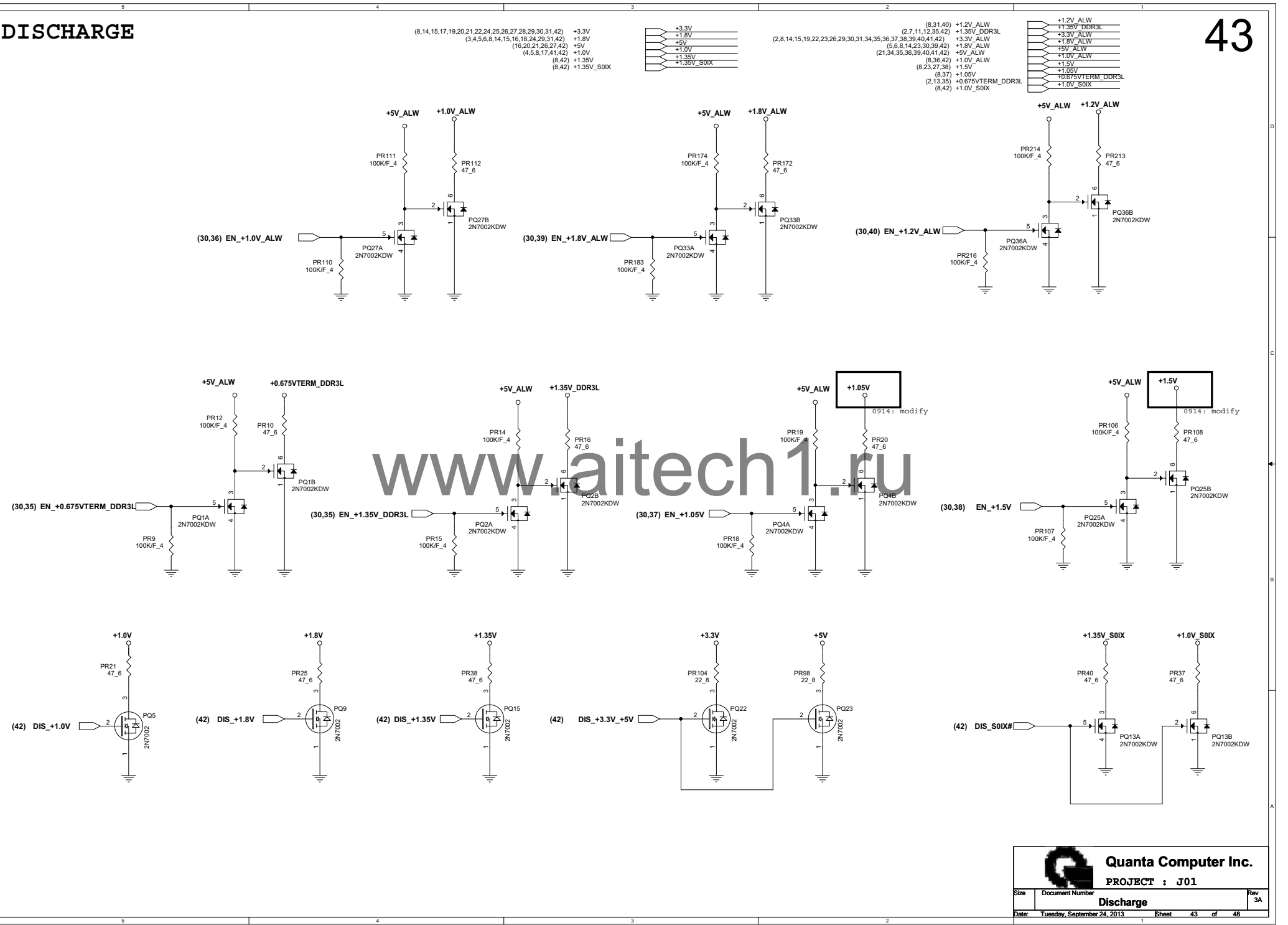
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PC116

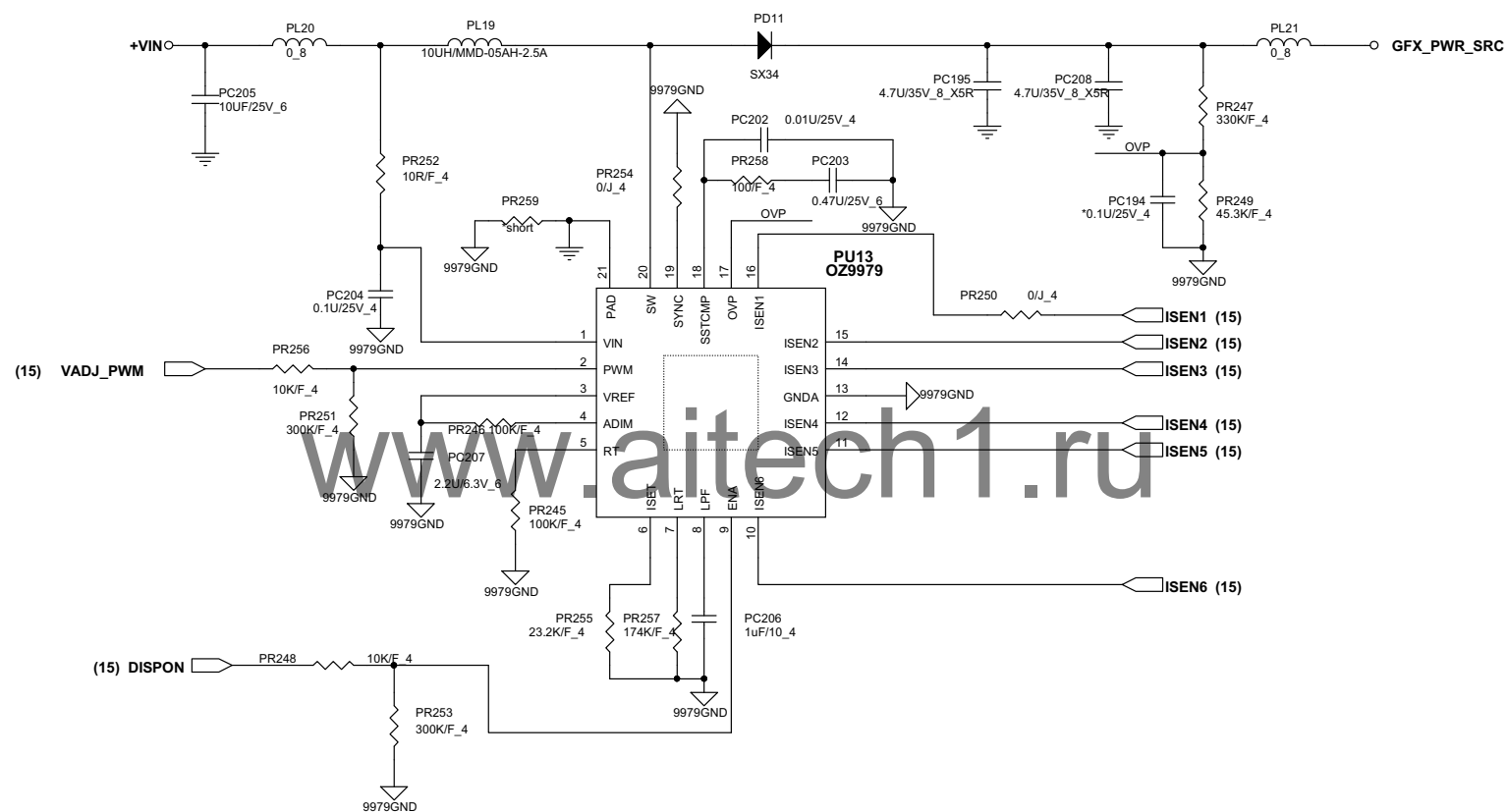




DISCHARGE



For AUO Panel



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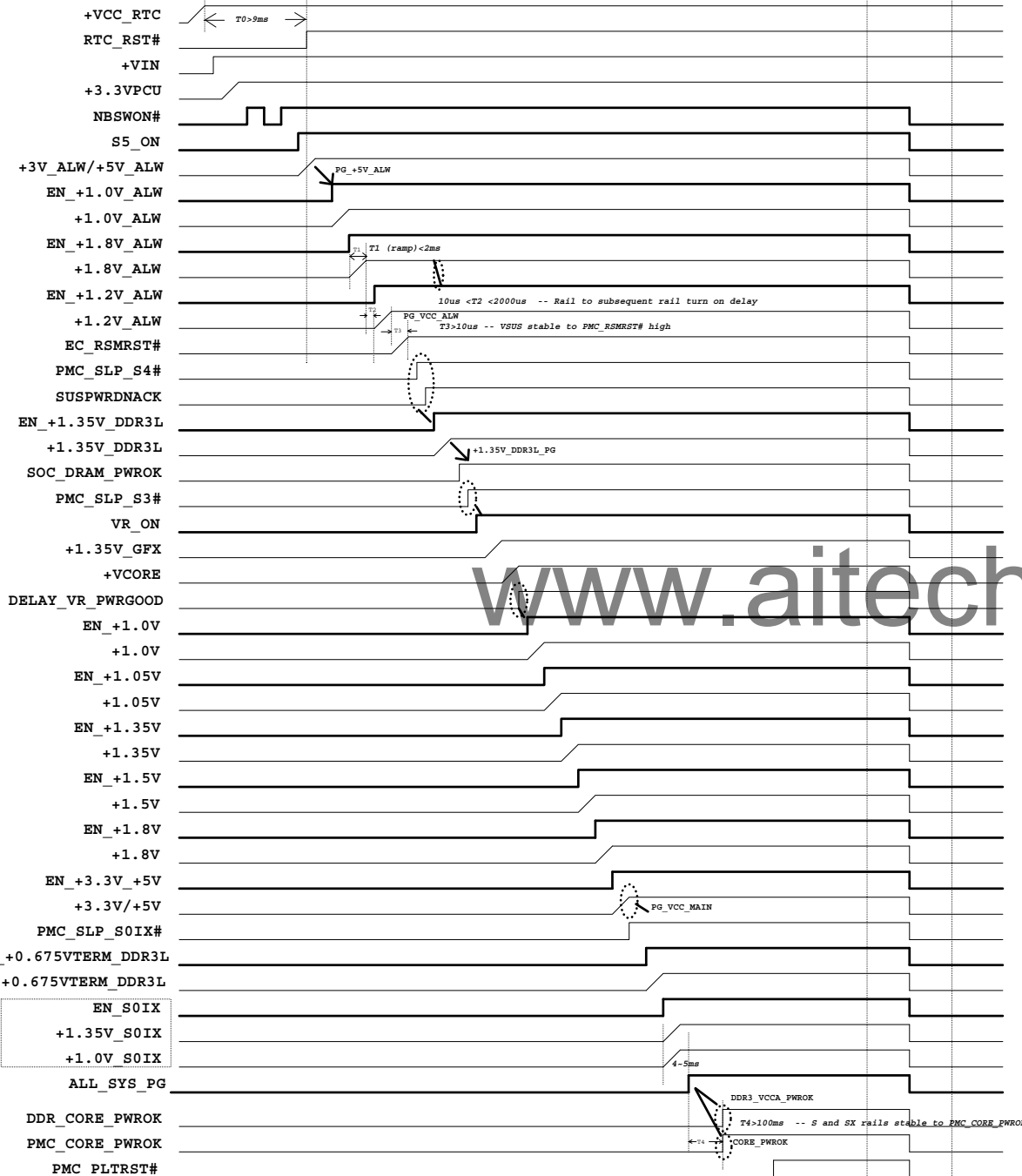
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		3A

Back light (OZ9979)

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Power on sequence OFF

45



T0: +RTCVCC stable to RTCRST# high > 9ms
T1: VR ramp up time from 10% to 90% voltage level < 2ms
T2: Rail to subsequent rail turn on delay < 2ms
T3: +VALWAS stable to EC_RSMRST# high > 10us
T4: +VS rails stable to PMC_CORE_PWROK > TBD

NOTE:


1. T1 and T2 are recommended time for all the VR rails unless specified otherwise. The VR ramp up time T2 and subsequent rail delay T3 are put in place to avoid inrush current which may be caused by multiple loads turning on simultaneously or fast charging of VR output decoupling.

2. Platform devices other than SOC sequencing are not explicitly shown as they are not limited by the SOC sequencing requirement.

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Green signals (PG) to EC
Blue timing -- Intel
Pink signals from EC

Model		REV	CHANGE LIST			MODEL	FROM	To								
	3A	<div>B2-->C</div> <div>1. Depopulate related components in the debug LED circuit.</div> <div>2. Modify power name for discharging ciurcit</div> <div>3. Modify PD5/PD6 footprint</div>	<div>www.aitech1.ru</div>													
						DOC NO.		PROJECT MODEL :		PD7	APPROVED BY:				DATE: 2011/10/28	
								PART NUMBER:			DRAWING BY:				REVISION: 1A	



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Change History2

Size


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Document Number

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3A

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